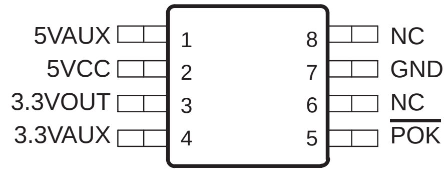
- **Automatic Input Voltage Source Selection**
- **Glitch-Free Regulated Output**
- **5-V Input Voltage Source Detector With Hysteresis**
- **400-mA Load Current Capability With 5-V or 3.3-V Input Source**
- **Power OK Feature Based on Voltage Supervisor of 3.3VOUT**
- **Low $r_{DS(on)}$ Auxiliary Switch**
- **Thermally Enhanced PowerPAD™ Packaging Concept for Efficient Heat Management**

DGN PACKAGE
(TOP VIEW)



NC – No connect

description

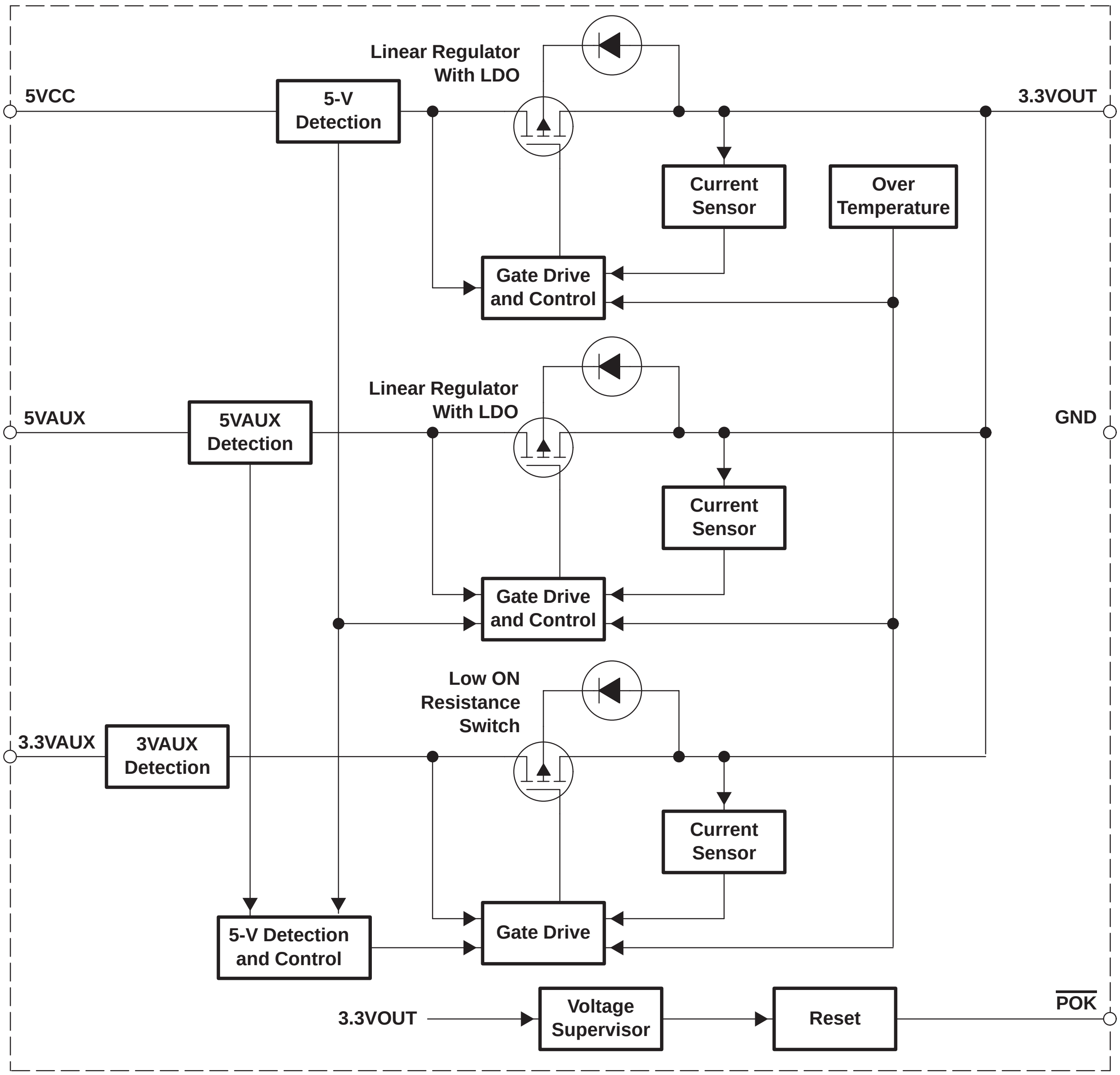
The TPPM0302 is a low-dropout regulator with auxiliary power management that provides a constant 3.3-V supply at the output capable of driving a 400-mA load.

The TPPM0302 provides a regulated power output for systems that have multiple input sources and require a constant voltage source with a low-dropout voltage. This is a single output, multiple input, intelligent power source selection device with a low-dropout regulator for either 5VCC or 5VAUX inputs, and a low-resistance bypass switch for the 3.3VAUX input.

Transitions may occur from one input supply to another without generating a glitch, outside of the specification range, on the 3.3-V output. The device has an incorporated reverse blocking scheme to prevent excess leakage from the input terminals in the event that the output voltage is greater than the input voltage. The output voltage is continually monitored for constant output, and any deviation from the internal set limit (≈2.8 V) is reported by a low signal on the $\overline{\text{POK}}$ output.

The input voltage is prioritized in the following order: 5VCC, 5VAUX, and 3.3VAUX.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3.3VAUX	4	I	3.3-V auxiliary input
3.3VOUT	3	O	3.3-V output with a typical capacitance load of 4.7 µF
5VAUX	1	I	5-V auxiliary input
5VCC	2	I	5-V main input
GND	7	I	Ground
NC	6, 8	I	No internal connection
$\overline{\text{POK}}$	5	O	Power OK

Table 1. Input Selection

INPUT VOLTAGE STATUS (V)			INPUT SELECTED	OUTPUT (V)	OUTPUT (I)
5VCC	5VAUX	3.3VAUX	5VCC/5VAUX/3.3VAUX	3.3VOUT	I_L (mA)
0	0	0	None	0	0
0	0	3.3	3.3VAUX	3.3	375
0	5	0	5VAUX	3.3	400
0	5	3.3	5VAUX	3.3	400
5	0	0	5VCC	3.3	400
5	0	3.3	5VCC	3.3	400
5	5	0	5VCC	3.3	400
5	5	3.3	5VCC	3.3	400

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, 5-V main input, $V_{(5VCC)}$ (see Notes 1 and 2) . . . . . 7 V
Auxiliary voltage, 5-V input, $V_{(5VAUX)}$ (see Notes 1 and 2) . . . . . 7 V
Auxiliary voltage, 3.3-V input, $V_{(3.3VAUX)}$ (see Notes 1 and 2) . . . . . 5 V
3.3-V output current limit, $I_{(LIMIT)}$ . . . . . 1.5 A
Continuous power dissipation, P_D (see Note 3) . . . . . 1.36 W
Electrostatic discharge susceptibility, human body model, $V_{(HBMESD)}$ . . . . . 2 kV
Operating ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C
Operating junction temperature range, T_J . . . . . –5°C to 120°C
Lead temperature (soldering, 10 second), $T_{(LEAD)}$ . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Absolute negative voltage on these terminal should not be below –0.5 V.
3. Refer to the Thermal Information Section.

recommended operating conditions

	MIN	TYP	MAX	UNIT
5-V main input, $V_{(5VCC)}$	4.5		5.5	V
5-V auxiliary input, $V_{(5VAUX)}$	4.5		5.5	V
3.3-V auxiliary input, $V_{(3.3VAUX)}$	3		3.6	V
Load capacitance, C_L	4.23	4.7	5.17	µF
Load current, I_L	0		400	mA
Ambient temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, T_A = 0°C to 70°C, C_L = 4.7 μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(5VCC)}$/ $V_{(5VAUX)}$	5-V inputs		4.5	5	5.5	V
$I_{(Q)}$	Quiescent supply current	From 5VCC or 5VAUX terminals, I_L = 0 mA to 400 mA		2.5	5	mA
		From 3.3VAUX terminal, I_L = 0 A		250	500	μA
I_L	Output load current		0.4			A
$I_{(LIMIT)}$	Output current limit	3.3VOUT = 0 V		1	1.5	A
$T_{(TSD)}$†	Thermal shutdown	3.3VOUT output shorted to 0 V	150		180	°C
T_{hys}†	Thermal hysteresis			15		
$V_{(3.3VOUT)}$	3.3-V output	I_L = 400 mA	3.135	3.3	3.465	V
C_L	Load capacitance	Minimal ESR to insure stability of regulated output		4.7		μF
$I_{lkg(REV)}$	Reverse leakage output current	Tested for input that is grounded. 3.3VAUX, 5VAUX, or 5VCC = GND, 3.3VOUT = 3.3 V			50	μA

† Design targets only. Not tested in production.

5-V detect

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TO\_LO)}$	Threshold voltage, low	5VAUX or 5VCC↓	3.85	4.05	4.25	V
$V_{(TO\_HI)}$	Threshold voltage, high	5VAUX or 5VCC↑	4.1	4.3	4.5	V

auxiliary switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(SWITCH)}$	Auxiliary switch resistance	5VAUX = 5VCC = 0 V, 3.3VAUX = 3.3 V, I_L = 150 mA			0.4	Ω
$\Delta V_{O(\Delta VI)}$	Line regulation voltage	5VAUX or 5VCC = 4.5 V to 5.5 V		2		mV
$\Delta V_{O(\Delta IO)}$	Load regulation voltage	20 mA < I_L < 400 mA		40		mV
$V_I - V_O$	Dropout voltage	I_L < 400 mA			1	V

Power OK ($\overline{POK}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TO\_POK)}$	POK threshold voltage	3.3VOUT = 0 → 3.3 V and starts $\overline{POK}$ delay timer	2.67	2.8	2.93	V
V_{OL}	Output low voltage				0.4	
I_{OH}	Output high current				200	μA
V_{OH}	Output high voltage	5K pullup to 3.3VOUT		3.3		V

timing characteristics, T_A = 0°C to 70°C, C_L = 4.7 μF (unless otherwise noted)†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Power OK delay	5VCC or 5VAUX or 3.3VAUX > V_{TO} and $\overline{POK}$ ↑		5	10	ms

† Design targets only. Not tested in production.

thermal characteristics‡

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal impedance, junction-to-case		4.7		°C/W
$R_{\theta JA}$	Thermal impedance, junction-to-ambient		59		°C/W

‡ Based on Texas Instrument recommended board for PowerPAD package.

PARAMETER MEASUREMENT INFORMATION

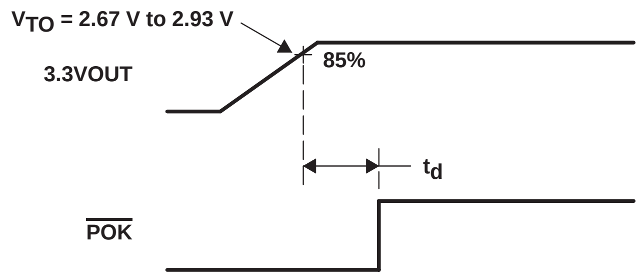


Figure 1. Power OK Timing Diagram

TYPICAL CHARACTERISTICS

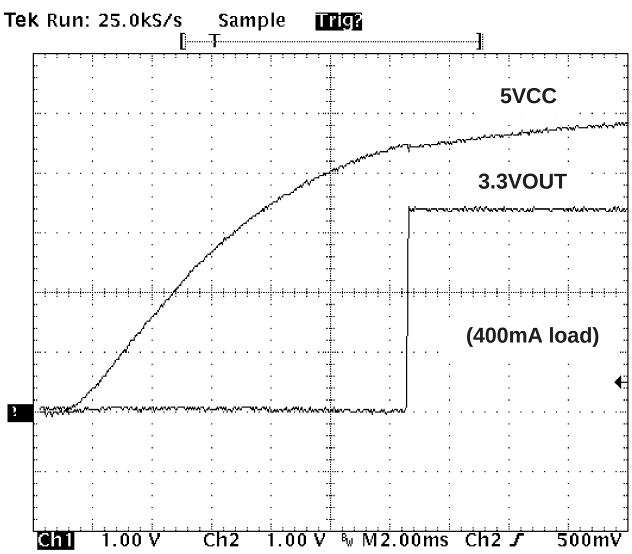


Figure 2. 5VCC Cold Start

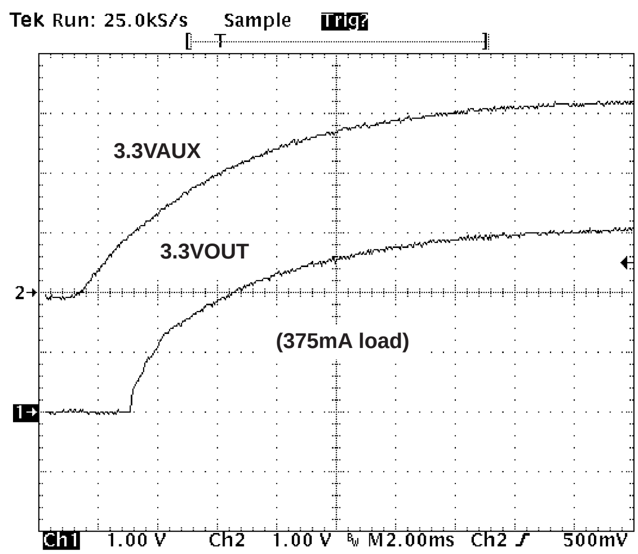


Figure 3. 3.3VAUX Cold Start

TYPICAL CHARACTERISTICS

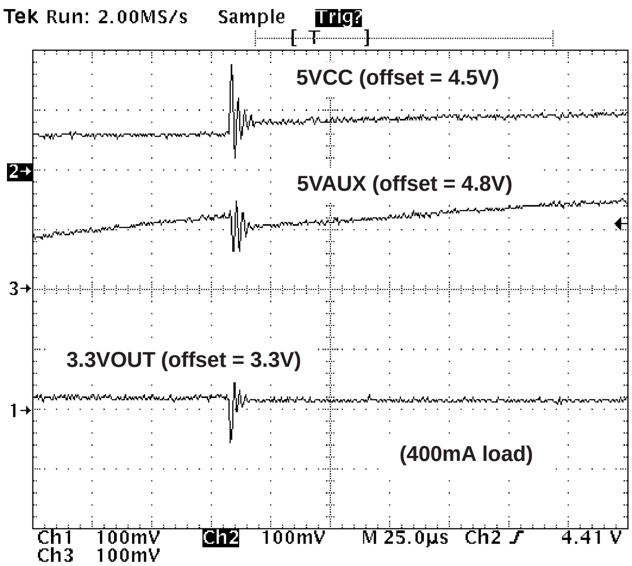


Figure 4. 5VCC Power Up (5VAUX = 5 V)

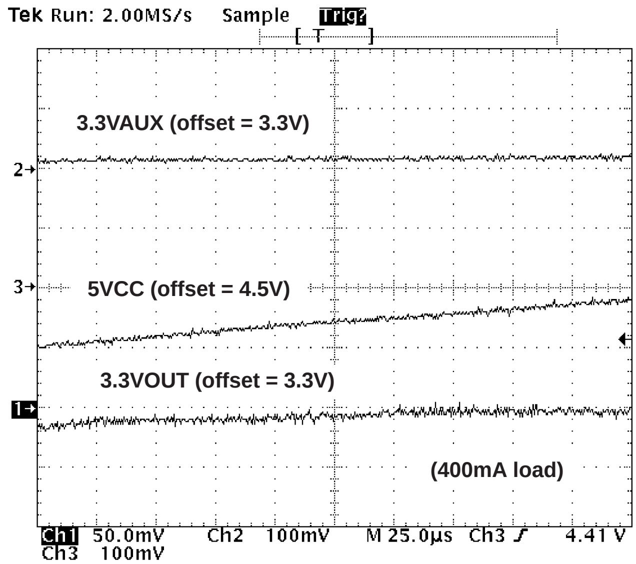


Figure 5. 5VCC Power Up (3.3VAUX = 3.3 V)

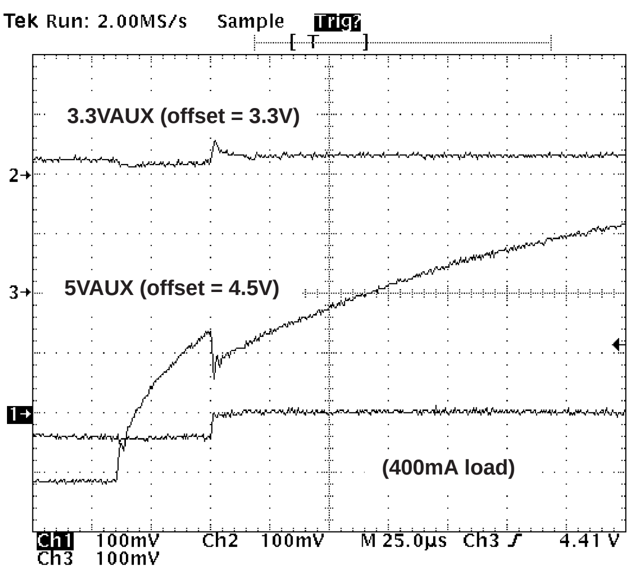


Figure 6. 5VAUX Power Up (3.3VAUX = 3.3 V)

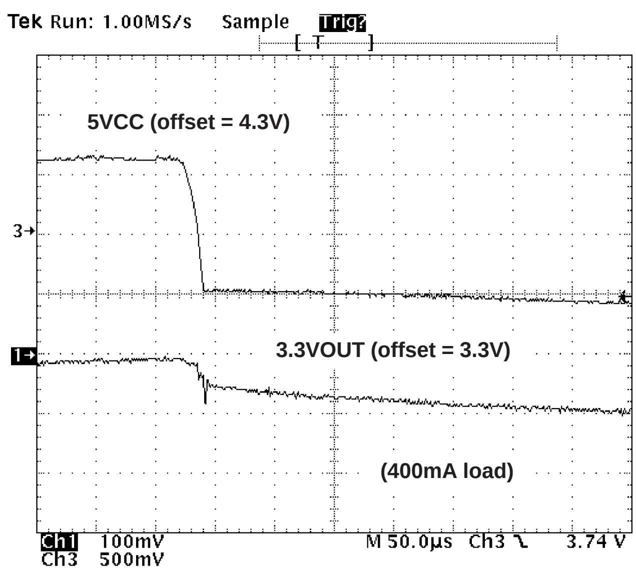


Figure 7. 5VCC Power Down (3.3VAUX = 3.3 V)

TYPICAL CHARACTERISTICS

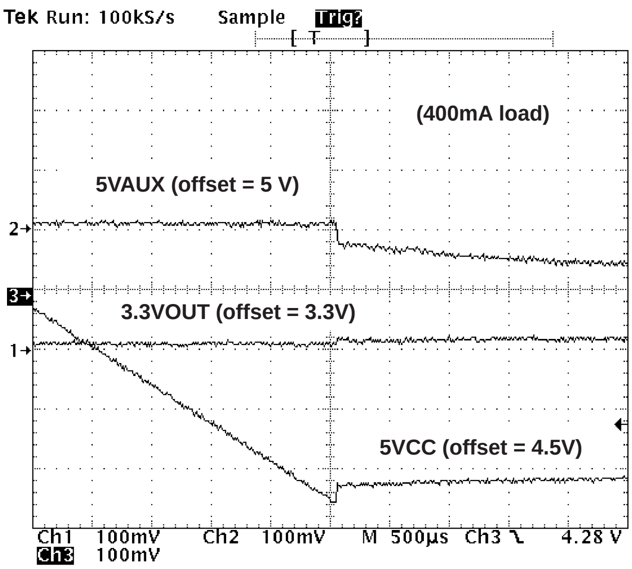


Figure 8. 5VCC Power Down (5VAUX = 5 V)

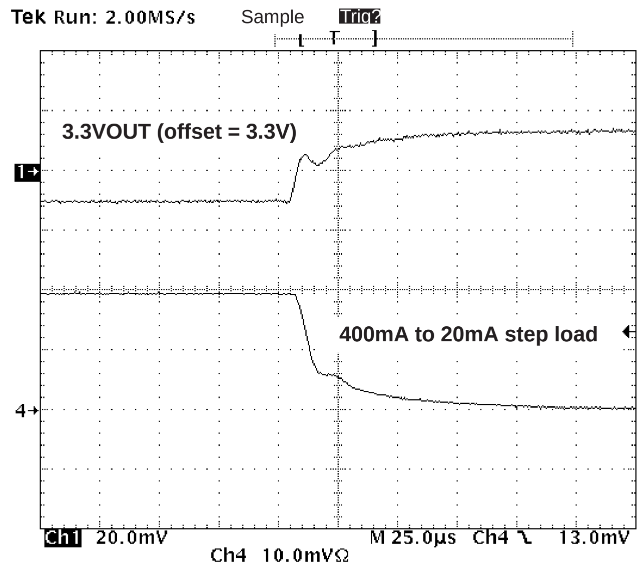


Figure 9. 5VCC Load Transient Responses Falling

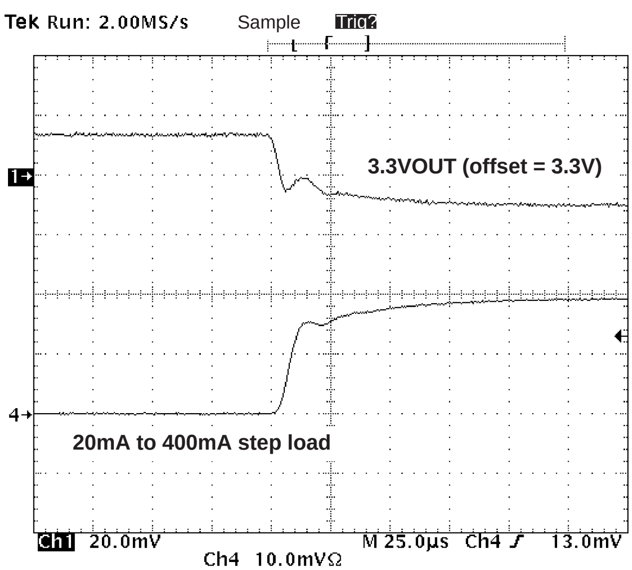


Figure 10. 5VCC Load Transient Response Rising

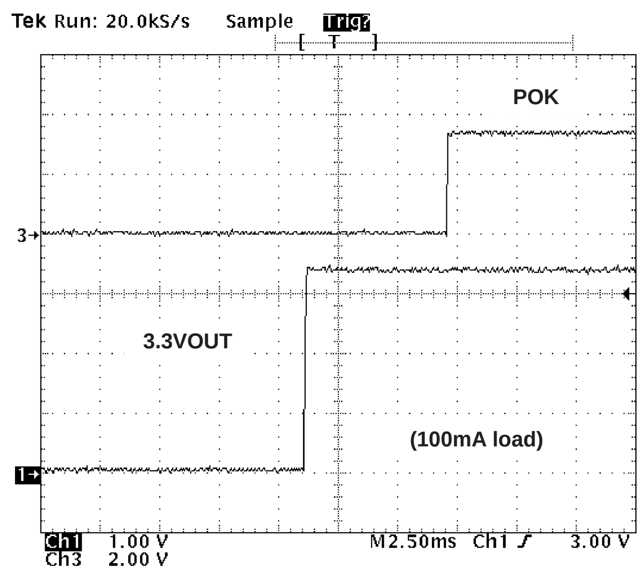


Figure 11. 5VCC Cold Start, $\overline{\text{POK}}$ Released

THERMAL INFORMATION

To ensure reliable operation of the device, the junction temperature of the output device must be within the safe operating area (SOA). This is achieved by having a means to dissipate the heat generated from the junction of the output structure. There are two components that contribute to thermal resistance. They consist of two paths in series. The first is the junction to case thermal resistance, $R_{\theta JC}$; the second is the case to ambient thermal resistance, $R_{\theta CA}$. The overall junction to ambient thermal resistance, $R_{\theta JA}$, is determined by:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

The ability to efficiently dissipate the heat from the junction is a function of the package style and board layout incorporated in the application. The operating junction temperature is determined by the operating ambient temperature, T_A, and the junction power dissipation, P_J.

The junction temperature, T_J, is equal to the following thermal equation:

$$T_J = T_A + P_J\,(R_{\theta JC}) + P_J\,(R_{\theta CA})$$

$$T_J = T_A + P_J\,(R_{\theta JA})$$

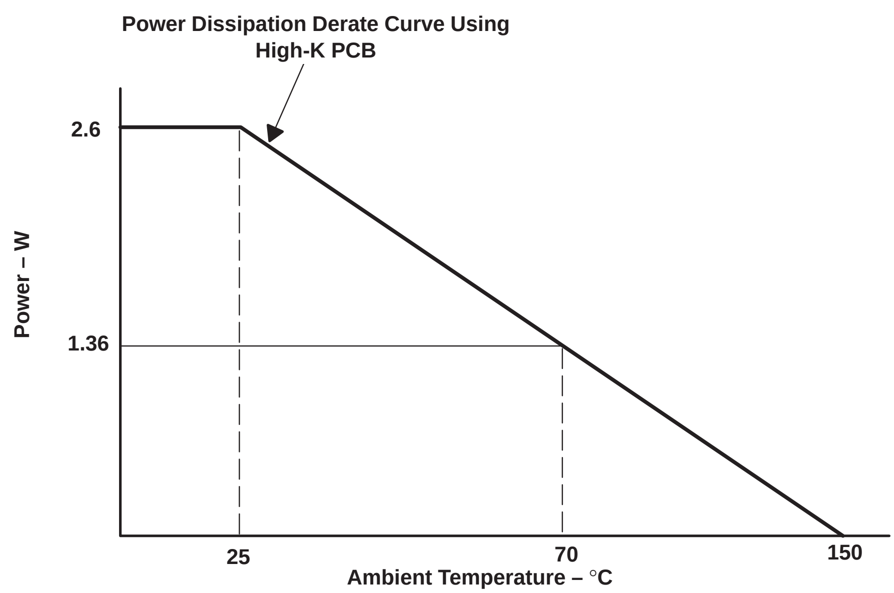
This particular application uses the 8-pin DGN PowerPAD package with a standard lead frame with dedicated ground terminal. Using a multilayer printed-circuit board (PCB), the power pad is mounted as recommended in the TI packaging application. The power pad is electrically connected to the ground plane of the circuit board through the dedicated ground pin and the die mount power pad. This will provide a means for heat spreading through the copper plane associated within the PCB (GND Layer). This concept could provide a thermal resistance from junction to ambient, $R_{\theta JA}$, of 59°C/W if implemented correctly.

Hence, maximum power dissipation allowable for an operating ambient temperature of 70°C, and a maximum junction temperature of 150°C is determined as:

$$P_J = (T_J – T_A) / R_{\theta JA}$$

$$P_J = (150 – 70) /59 = 1.36 \text{ W}$$

Using a multilayer board and utilizing the ground plane for heat spreading.



NOTE: This curve is to be used for guideline purposes only. For a particular application, a more specific thermal characterization is required.

Figure 12. Power Dissipation Derating Curve

APPLICATION INFORMATION

packaging

To maximize the efficiency of this package for application on a single layer or multilayer PCB, certain guidelines must be followed.

The following information is to be used as a guideline only. For further information, refer to the PowerPAD concept implementation document.

multilayer PCB

Guidelines for mounting the PowerPAD IC on a multilayer PCB with a ground plane.

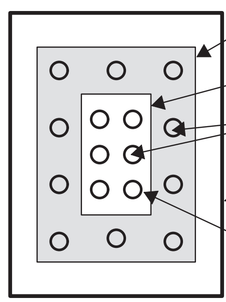


Figure 13. Package and Land Configuration for a Multilayer PCB

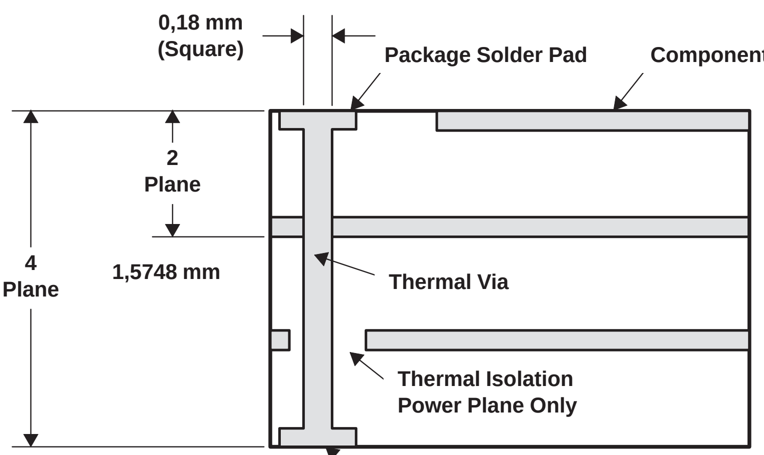


Figure 14. Multilayer Board (Side View)

APPLICATION INFORMATION

In a multilayer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors (die area, number of thermal vias, thickness of copper) Consult the *PowerPAD Thermally Enhanced Package Technical Brief.*

single-layer PCB

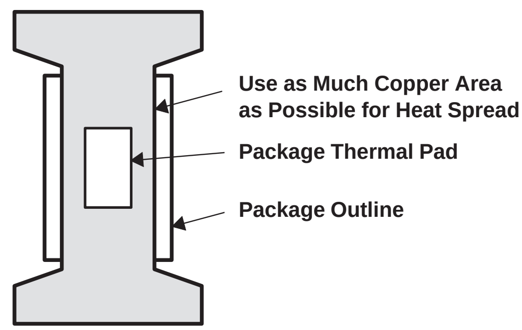


Figure 15. Land Configuration for Single-layer PCB

Layout recommendations for a single-layer PCB utilize as much copper area as possible for power management.

In a single layer board application, the thermal pad is attached to a heat spreader (copper area) by using low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above, it is advisable to use as many copper traces as possible to dissipate the heat.

IMPORTANT

If the attachment method is NOT implemented correctly, the functionality of the product is not efficient. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.

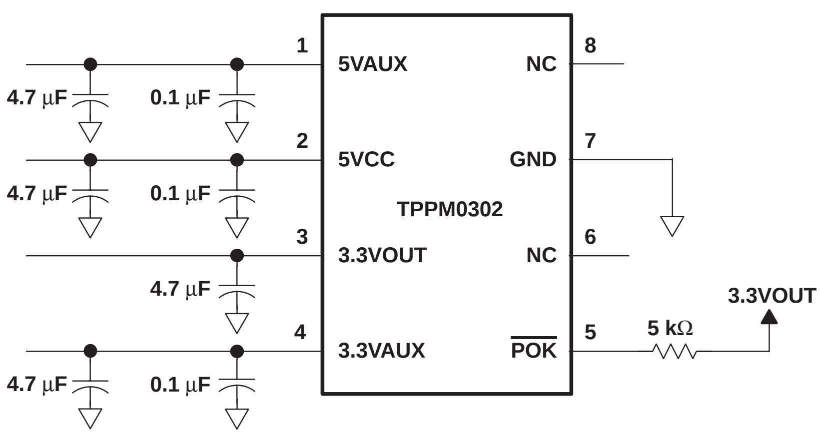
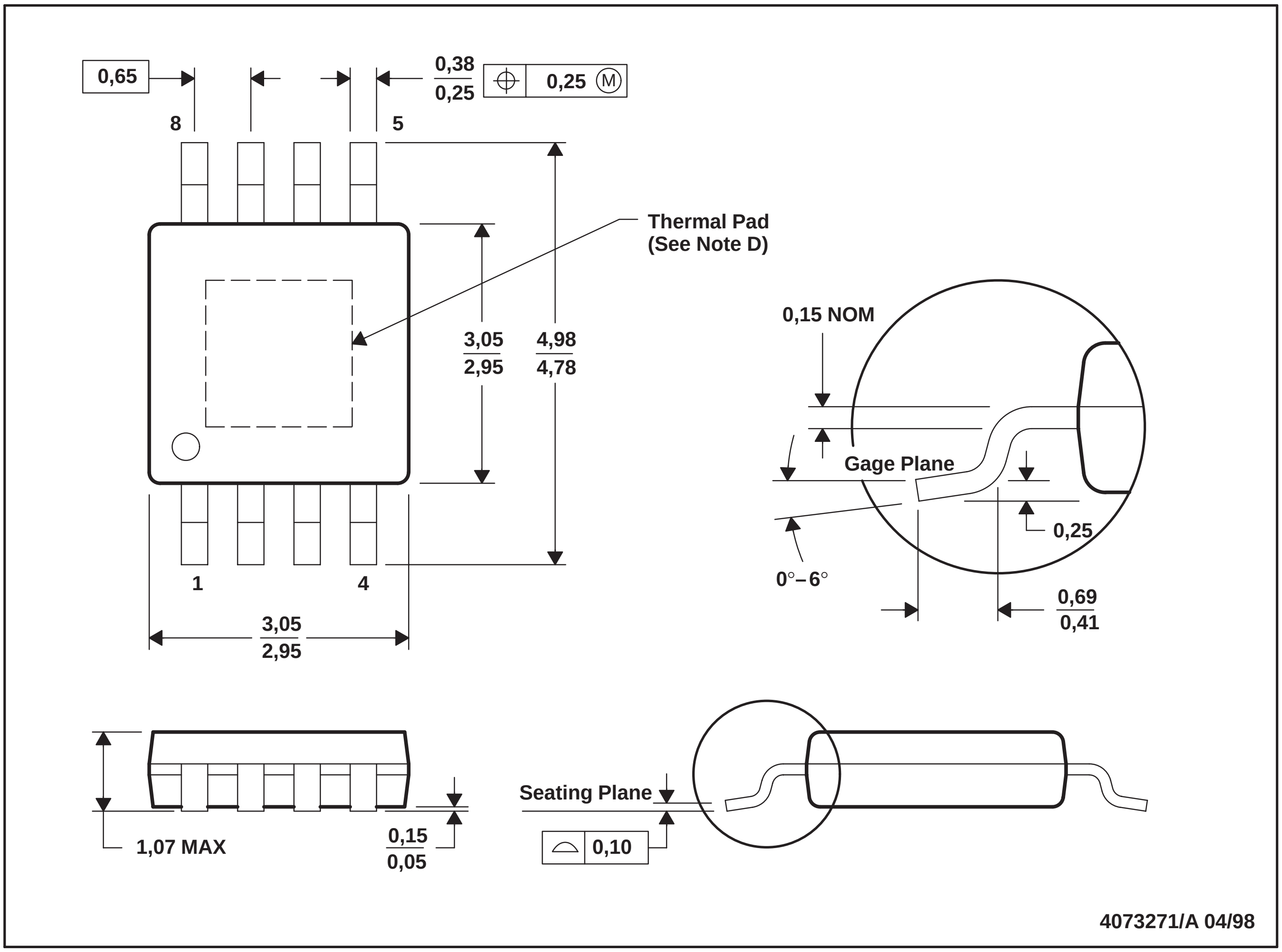


Figure 16. Typical Application Schematic

MECHANICAL DATA

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly to selected leads.
E. Falls within JEDEC MO-187

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Logic	logic.ti.com	Military	www.ti.com/military
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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPPM0302DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPPM0302DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPPM0302DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPPM0302DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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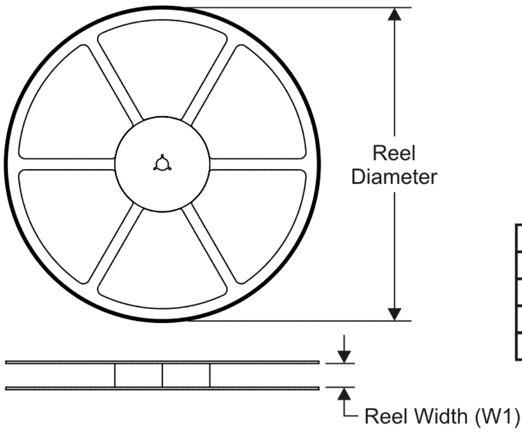
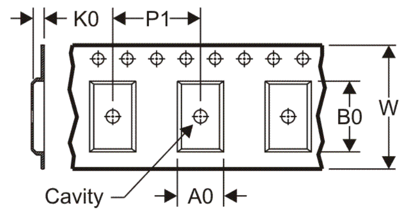
TAPE AND REEL INFORMATION

REEL DIMENSIONS

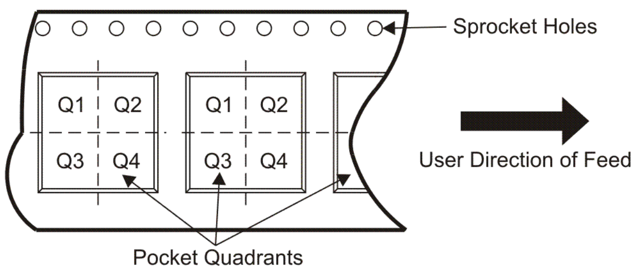


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

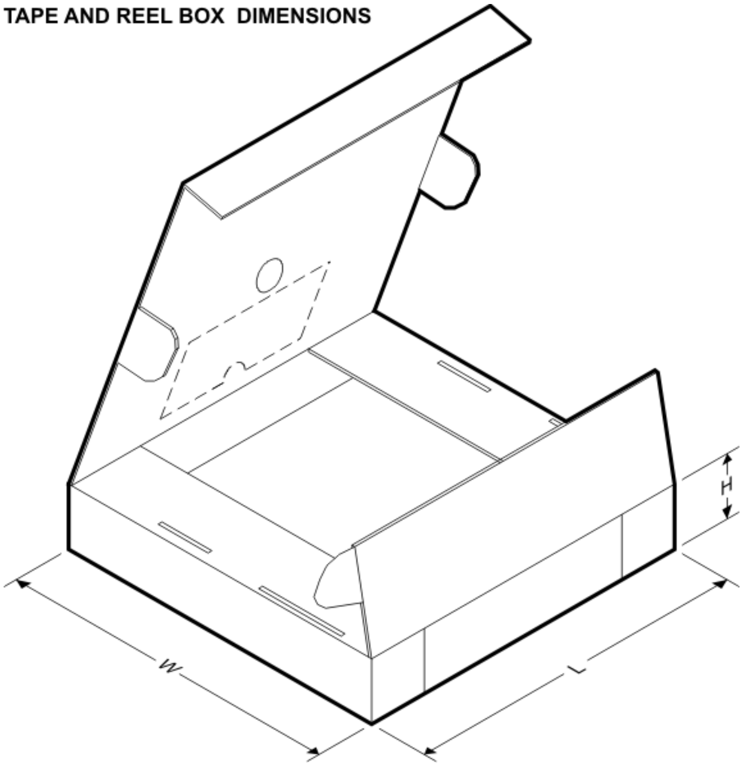
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPPM0302DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

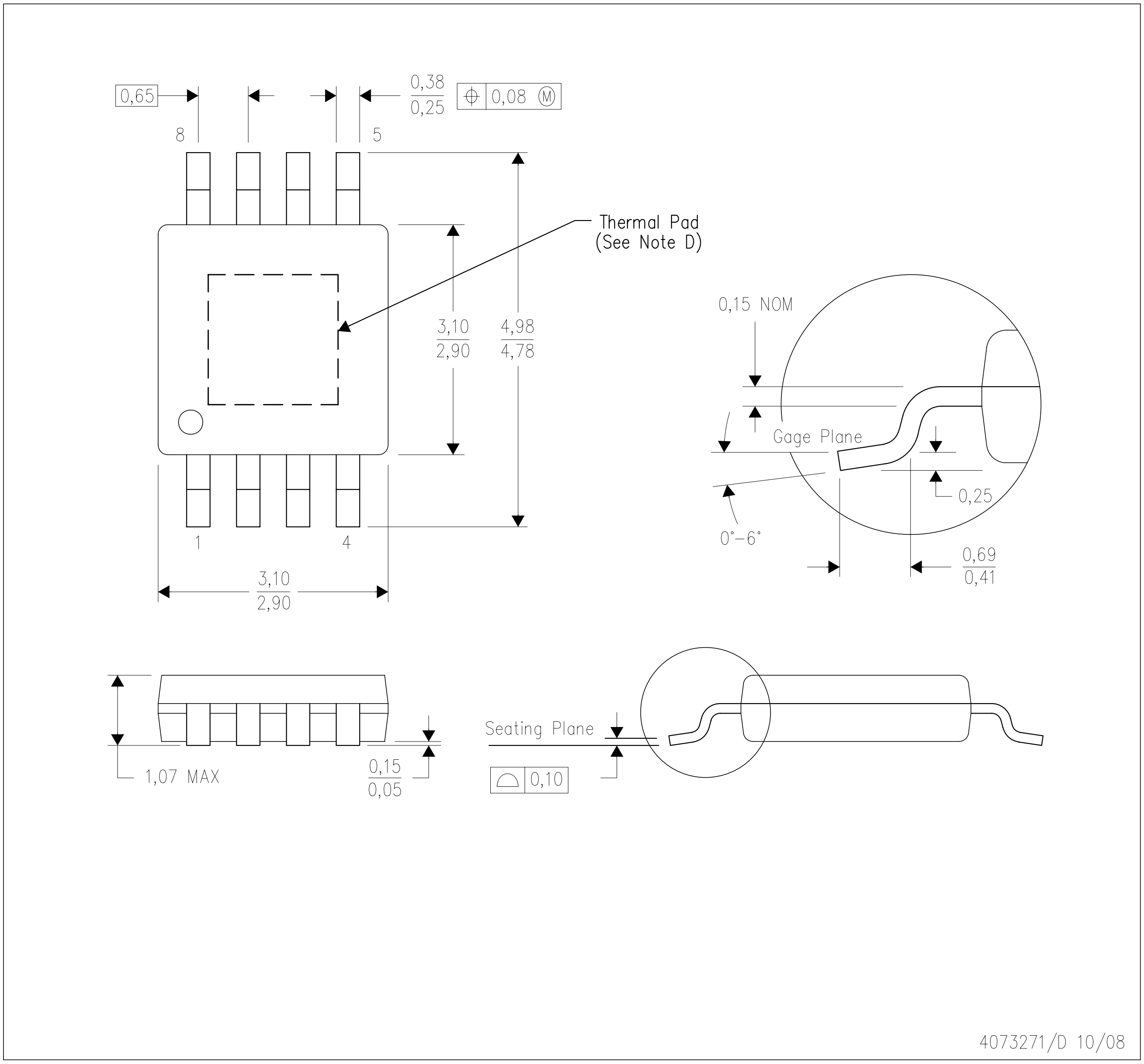
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPPM0302DGNR	MSOP-PowerPAD	DGN	8	2500	346.0	346.0	29.0

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MO-187

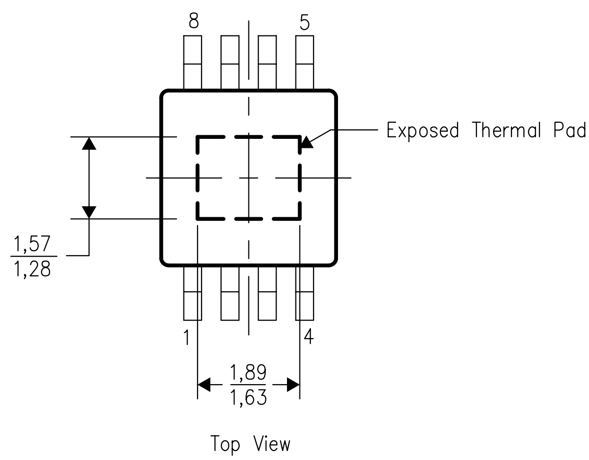
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

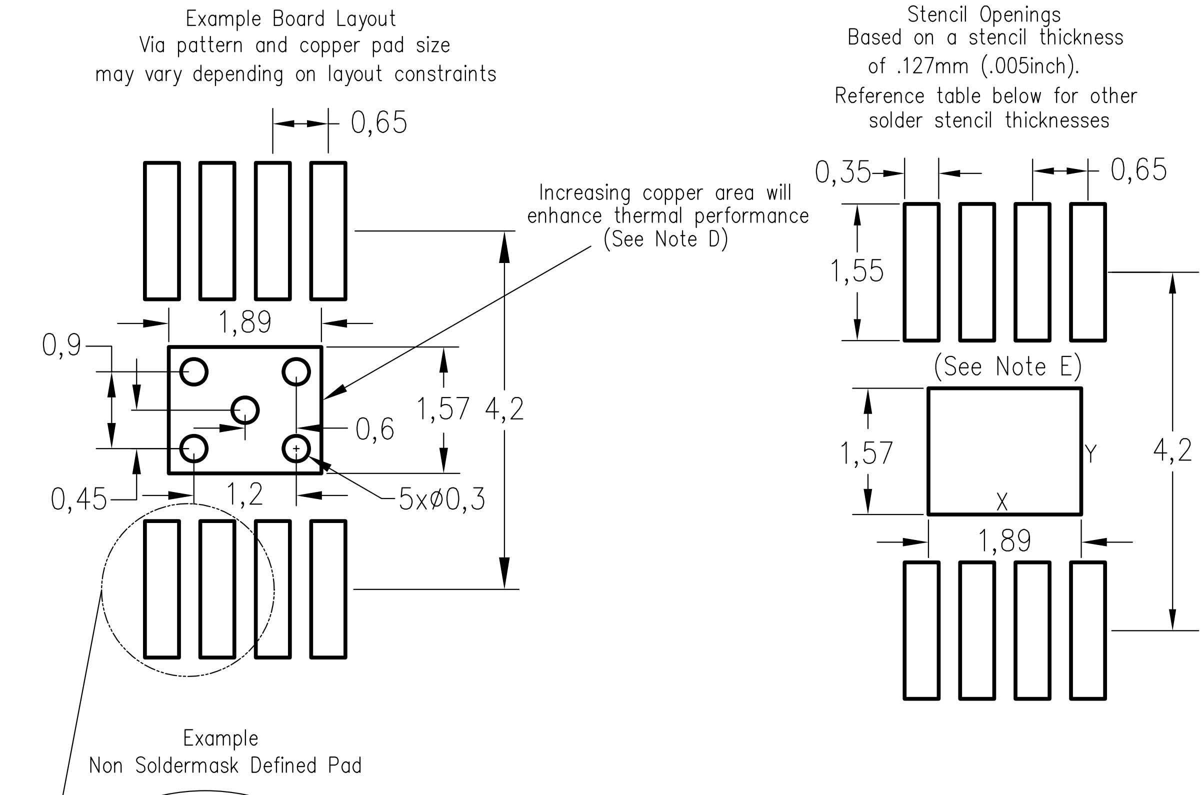
The exposed thermal pad dimensions for this package are shown in the following illustration.

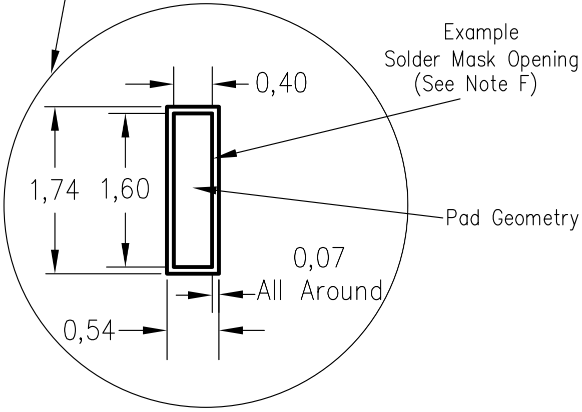


NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGN (R-PDSO-G8) PowerPAD™





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737-2/C 10/07

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
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